64 KILOBYTE DYNAMIC RAM CARD

with

PROGRAMMABLE GRAPHICS

CONTENTS

- - - - - - - - - - - - - - -

MICRO POWER

8/8A, REGENT STREET,
CHAPEL ALLERTON, LEEDS
LS7 4PE

CONSTRUCTION NOTES

Please read the accompanying notes and manual carefully before you start to build the board.

You will need a soldering iron with a very fine bit as many of the solder pads are close together. It is essential to check that each component is inserted correctly before you solder it. This is particularly important if you decide to build the board without using IC sockets, as it is difficult to remove ICs from a board without damaging the printed circuit tracks.

All the components should be easy to obtain, with the possible exception of FR1, which is a 15 x 4K7 DIL resistor pack to pull up certain of the Nasbus lines to +5v. If this device is not available, it could be replaced by 14 separate 1/8 watt resistors (one of the resistors in the pack is unused); alternatively, several manufacturers, including Radiospares, produce a 13 x 4K7 pack which could be used with a single discrete resistor. If an alternative device is used you may have to change the pin connected to +5v, which at present is pin 1.

Most of the TTL chips are Low-power Schottky types (LS), but for those marked S, you must use standard Schottky or Advanced Low-power Schottky (ALS) chips.

The four tantalum decoupling capacitors on the memory section must be mounted so that for C1 and C2 the positive side is to the top of the board, and for C20 and C22 the positive side is to the bottom. Note that C30 will not normally be required; if it is necessary to provide a delay on the CAS signal only a small value will be required - do not use a 0.1 uF decoupling capacitor.

The two small pads near to pad B between M32 and F5, which are separated by a track running across the board to pin 14 of F5, should be connected by a wire link; carefully remove the resist on the component side of the holes and solder a short length of wire between them. Pad S between F3 and F4 has been incorrectly marked. The correct pad is the one to the lower left of the marked pad.

If you are using the card with a Nascom 2 you will not need components G11 and G12 and the Buffer section. The buffer section can be cut off and discarded if you wish, but you must leave at least one row of plated through holes on the edge connector, as these form an essential electrical path between the two sides of the board.

For the Nascom 2 pin 1 of M39 should be tied to ground. To do this, disconnect the chip from IMEM by cutting the track from pin 1 on the component side of the board or by breaking the connection at the plated through hole with a small sharp twist drill. Connect pin 1 of M39 to ground on the adjacent decoupling capacitor, C25. Also on the Nascom 2 the RAM inhibit line (RAMDIS, Nasbus line 9) should be pulled up to +5 v with a resistor of approximately 560 Ohms.

COMPONENTS LIST

Memory and Memory Mapper

Integrated Circuits

M1-M32	4116 200 nsec	M33	74LS245
M34,M38,M43	74LS240	M35,M36	74LS240
M37	74LS08	M39	74LS139
M40,M45	74LS158	M41,M42	74LS74
M44	74LS75	M46,M47	74LS04
F1	74S22/74ALS22	F2	74S00/74ALS00
F3,F4	74S30/74ALS30	F8,F9	74S138/74ALS138

F6,F7 DIL sockets for decode headers

Capacitors

C1,C2,C20,C22	4.7 uF,16V Tantalum
C3-C29	0.1 uF disc ceramic
C30	See text.
C31	220 uF,16V, Electrolytic
C32,C33	100 uF, 25V, Electrolytic

Resistors

R1-R16	33 Ohm
R17	1kOhm
FR1	15x4k7 resistor pack

Graphics Section

Integrated Circuits

G1,G3	2x4118, or 6116, or 2716	G2	74LS245
G4,G12*	74LS244	G5,G8,G9	74LS157
G6	74LS04	G7	74LS132

G10,G11* 24 pin DIL sockets

Buffer Section*

Integrated Circuits

B1,B10	74LS00	B2	74LS244
B3	8K Basic ROM (Optional)	B4	A 74LS156
B5,B6,B12	74LS74	B7	74LS367
B8	74LS257	B9	Power-on decode links
B11	74S86	B13	74132
B14	74LS221	B15,B16,B17,B1	74LS245
B19	7407	B20	74S04
Diode D1	1N4148 or equivalent		

Resistors

R101,R107,R108,R111,R112,R113,R114,R115,R124	1KO
R102,R103,R104,R105,R106,R116,R122,R134,R135	2K2
R109,R117	4K7
R110,R118,R119,R120,R121,R123,R130,R131,R132,R133	10K

Capacitors

All decoupling capacitors are 0.1 uF, disc ceramic

---

* G11,G12 and the buffer section are not required for the Nascom 2.

---

64 KILOBYTE DYNAMIC STORE AND PROGRAMMABLE GRAPHICS FOR NASCOM

INTRODUCTION

The glass-fibre p.c.b. is double sided, with interconnections via plated-through holes. Its dimensions are 304mm (12ins) by 203mm (8ins).

The design allows for up to four blocks of 16KB dynamic store. The 64K address field is mappable in 4K blocks by use of links and, by use of an array of uncommitted logic, any two 4K blocks can be further divided into 2K blocks.

The programmable graphics section is entirely separate from the dynamic store but can be mapped-in and uses ROM and/or RAM.

The board is divided into two potentially separate physical parts so as to allow its use with NASCOM 1 or NASCOM 2 processor boards. For NASCOM 1 it provides buffering facilities, power-on/reset logic for dynamic store and an 8K BASIC ROM socket on the 203mm (8ins) by 101mm (4ins) "buffer" section. The output 77-way connector provides the 80-BUS (NASBUS) interface. Note that the connector actually has 78 ways when the keyway is included.

Referring to Fig.1, the central connector is the junction between the store board proper and the NASCOM 1 buffer board. NASCOM 2 applications require separation of the two sections at this junction, the "buffer" section being discarded.

CONSTRUCTION

Physical Arrangements for NASCOM 1 - Fig.2

There are many possible arrangements of the processor and store boards. The two most commonly used are illustrated in Fig.2.

Separating the Boards

Separation of the two sections must be done with great care and is best tackled as follows:

First, scribe an accurate line along the connector pads on both sides to divide the 12inch length of the board into a 4" and 8" section. Place the board between two thin pieces of wood along the intended line of cut and clamp the whole assembly between two pieces of L-shaped aluminium, in a vice. Cut carefully along the aluminium guide with the finest sharp hacksaw or razorsaw available. The important point is to prevent the copper fingers of the edge connector separating from the fibre-glass substrate during the sawing action.

NASCOM 1 Edge Connector

The smaller edge connector on Fig.1 is pin-compatible with the NASCOM 1 43-way connector which is a raw Z80 interface and may, therefore, allow any Z80 based machine to be wired appropriately, giving 80-BUS (NASBUS) capability.

Use of DIP Sockets

It is common practice for home-built equipment to use sockets throughout, but experience shows that this is rarely cost effective. RAM in particular is more reliable

if soldered directly onto the board. The motivation for using sockets appears to be ease of modifications (you can lift legs of DIL's) and fault finding (easily removed and replaced). Actually faults are sometimes caused by the sockets, so if you insist on using them, buy the best.

MOS Warning

Note that great care must be taken with 4116 RAM chips because they use MOS technology - static is the enemy, so preferably use inserting tools that short all the pins together when handling the RAM out of the anti-static storage tubes or materials, or at least do not wear man-made fibre clothes and do not touch the actual pins, instead, handle by the ends of the plastic, or ceramic, packages only!

64 KILOBYTE RAM AND CONTROL LOGIC - Fig.3

This diagram shows the 64KB dynamic-RAM block and its control logic. The only option available is the choice of the number of RAM chips fitted i.e. one, two, three or four 16K blocks.

The first 16K uses M1, M5, M9, M13, M17, M21, M25 and M29. The second block starts with M2, the third block with M3 and the fourth with M4.

The design centres around the 4116 200 nanosecond, or faster, dynamic store element. Slower RAM can be used but the subsequent timing cannot be guaranteed.

With all 64KB fitted, the whole of the Z80 address field is occupied by RAM. The mapper facility allows parts of this field to be selectively inhibited, in either Read or Write mode or both. The circuit itself is derived from a standard Mostek design, adapted for NASBUS. The front edge of the Memory Requested signal, $\overline{\text{MREQ}}$, is ignored until the first clock pulse appears, hence the Enable Row Address Strobe, ERAS, is generated synchronized to the first clock pulse after $\overline{\text{MREQ}}$, rather than with $\overline{\text{MREQ}}$ itself. ERAS is also routed to M41 to clock the logic which produces the signal AMX to enable the Address Multiplexers M40 and M45. The output from pin 4 of M40 actually generates the Column Address Select strobe, ECAS, hence is two gate delays later than in time with the Address Lines themselves. The capacitor C30 is not normally necessary. It delays ECAS and is used if, as a result of fast gates, ECAS is generated early, which manifests itself as corrupted data. Values from 22pf upwards, as required. The Row Address Select strobe, $\overline{\text{RAS}}$, is generated by the M34 gates. Now dynamic RAM requires to be refreshed on a regular basis but needs only the signal $\overline{\text{RAS}}$ to do this. The Z80 itself generates the refresh signal $\overline{\text{RFSH}}$ and also produces the necessary addresses to step round the rows in all RAM.

There are four $\overline{\text{RAS}}$ and four $\overline{\text{CAS}}$ signals generated, one for each block of 16K addresses.

THE MEMORY MAPPER - Fig.4

The memory mapper is split into two parts. Elements F8 and F9 provide a decode of the sixteen 4K blocks, available at F7, these are low-going signals for the selected 4K block valid during $\overline{\text{MREQ}}$, so that clean pulses are generated.

Element F5 provides a means of breaking down any two 4K blocks into 2K units. This is achieved by connecting one of the sixteen decodes annotated $\overline{\text{4KS0}}$, $\overline{\text{4KS1}}$ ..... $\overline{\text{4KSF}}$, to $\overline{\text{4KSX}}$ or $\overline{\text{4KSY}}$, thus producing $\overline{\text{2KSX0}}$ and $\overline{\text{2KSX1}}$ or $\overline{\text{2KSY0}}$ and $\overline{\text{2KSY1}}$, as appropriate.

The second part of the mapper logic allows the RAM to be selectively disabled via F2, F3 and F4. Any 4K or 2K decode may be linked as a "RAM INHIBIT READ" or as a "RAM INHIBIT WRITE" or as both.

The signals $\overline{\text{RIRA}}$ to $\overline{\text{RIRF}}$ inclusive, are RAM Inhibit Read A to F on F4 and $\overline{\text{RIWA}}$ to $\overline{\text{RIWF}}$ inclusive are RAM Inhibit Write A to F on F3.

For example, to inhibit RAM for the first 4K of the 64K address field in order to accommodate NAS-SYS, the 1K video map and the 1K user on-board RAM of the NASCOM 1, the following connections are made:

Connect $\overline{\text{4KS0}}$ on F7 pin 1 to	$\overline{\text{RIWA}}$ on F6 pin 1	(Inhibit Read)
	and $\overline{\text{RIRA}}$ on F6 pin 14	(Inhibit Write)
	also to $\overline{\text{CPUS1}}$ on F6 pin 7	(Enable NASCOM 1)
	and $\overline{\text{CPUS2}}$ on F6 pin 8	(Enable NASCOM 1)

Thus, when Read or Write is demanded in the first 4K, the dynamic store is inhibited on the 64KB board by the signal IMEM (Inhibit Memory) via F2 gates. Also, at F1, the NASCOM 1 on-board RAM is enabled by $\overline{\text{NASMEM}}$ via F2 and the signals $\overline{\text{CPUS1}}$ and $\overline{\text{CPUS2}}$. The authority for deciding whether the NASCOM 1 Z80 has access to its on-board memory is determined from outside the NASCOM 1, hence the need for the signal $\overline{\text{NASMEM}}$. The signals $\overline{\text{CPUS1}}$ and $\overline{\text{CPUS2}}$ are only used by a NASCOM 1 system. As shown above, the NASCOM 1 on-board ROM and RAM can be enabled only when the dynamic RAM is inhibited. However, there are circumstances in which the RAM may be inhibited without the processor board being enabled, for example with programmable graphics or the BASIC ROM. Enabling the NASCOM 1 processor board requires not only inhibiting RAM with a block decode but the decode must also be connected to a $\overline{\text{CPUS}}$ line. Two $\overline{\text{CPUS}}$ lines are provided and normally both will be connected to the same decode, however, it could prove desirable to use two separate 2K selects to accomplish more subtle facilities in particular cases. Note that NASCOM 1 has to be set up for external memory, i.e. EXT selected on the NASCOM 1 board.

Unlike the NASCOM 1, the NASCOM 2 itself decides whether some device external to itself is allowed to respond to an address. This is the opposite to the NASCOM 1 and is done by another signal called $\overline{\text{INHRAM}}$, (Inhibit RAM) on F1, F3 and F4. $\overline{\text{NASMEM}}$ is not used by NASCOM 2.

It is important that any unused pins on F2, F3 and F4 are pulled up to a logic "high" so that noise cannot affect the memory-enable signal $\overline{\text{NASMEM}}$ when no inhibit signals are present. This is done by the resistor pack at FR1.

NASCOM 1 BASIC ROM ADDRESSING

Nascom BASIC resides in the last 8K of the 64K addressable area of store, thus signals $\overline{\text{4KSE}}$ and $\overline{\text{4KSF}}$ on F7 pin 10 and 9 respectively, define this 8K area. These two signals connect to the Block Enable Links on B1 pins 1 and 2 on the buffer board and enable B3 for any address in the last 8K via the Read Enable signal $\overline{\text{REN}}$ (read only) via B1 pin 6 (see Fig.7).

The dynamic RAM in this area must be inhibited for Read operations by connecting $\overline{\text{4KSE}}$ to, say, $\overline{\text{RIRB}}$ and $\overline{\text{4KSF}}$ to $\overline{\text{RIRC}}$. To inhibit write operation is not strictly necessary for the ROM addressable area and if $\overline{\text{4KSE}}$ and $\overline{\text{4KSF}}$ are not connected to, say, $\overline{\text{RIWB}}$ and $\overline{\text{RIWC}}$ respectively, then Write can occur. By using extra logic, not supplied here, this facility can be used to operate a system where RAM resides

"behind" the BASIC ROM and can be written to by a BASIC "POKE" or "USR" subroutine and then accessed by, for example, a port output bit to switch off BASIC and enable RAM Read during another subroutine. The extra logic for an application such as this can conveniently make use of the four spare DIL positions shown at the top right-hand corner of Fig.1.

PROGRAMMABLE GRAPHICS - Fig 5

NASCOM 1 Implementation

NASCOM 1 boards mount the character generator chip MCM6576 as IC16 in a 24-pin DIP socket on the main board. This chip is removed, but handle it carefully as for MOS elements and put it in position G11 on the store board. To give interchangeability, use a 24-pin socket as on the original. It is now possible to pick up all the character generator signals from the NASCOM 1 board by using a pair of 24-pin flat-cable headers connected 1 to 1, 2 to 2 etc., between the NASCOM and store boards. This cable must be as short as is practicable and the physical arrangements shown earlier illustrates this cable routeing clearly. The DIP socket at G10 accepts these connections. This means that the character and row select signals are routed either to the character generator at G11 or to the devices at G3 or G1. The most significant address bit selects between G11 and G3/G1. Thus 2K of RAM can be fitted at G3/G1. This can consist of two 4118 (each 1K) or a single 6116 (each 2K) fitted at G3. The drawing (FIG.5) shows the connections for L1 and L2 when 4118 chips are fitted. For a 6116, L2 is disconnected from +5 volts and connected to G5 pin 12 and L1 is disconnected from G5 pin 12 and connected to G5 pin 4.

Under these conditions the G11 chip occupies the bottom 128 character positions and G3/G1 occupies the top 128 character positions as far as the system is concerned. Thus, if the video RAM sees the most-significant bit set, it accesses the appropriate row location for that character in G3/G1, and if the most significant bit is reset, it accesses the appropriate row location for that character at G11. To read or write to RAM at G3/G1, to or from the Z80, the whole of the RAM is mapped into the address field. The three multiplexers G5, G8 and G9 switch the RAM at G3/G1 between the address lines A11-A0 from the Z80 or the character-plus-row address from G10. The address lines A11 to A0 on G5, G8 and G9 must be wire linked to the prepared set of plated-through holes on the NASBUS connector identified BA11 to BA0, as indicated on Fig.1.

One location in the RAM at G3/G1 corresponds to a single row pattern of a character. In fact the rows are placed in sequence so the first character which is programmable occupies the first 16 locations of the G3/G1 RAM. The second character occupies the second 16 locations and so on. A single location is one byte and appears as a horizontal bit pattern in the character location on the screen if it is specified as that character. The least significant bit is on the left, and the most significant is on the right, of the displayed character. For NASCOM 1, link N1 should be made.

Read and Write to Graphics RAM

The two signals $\overline{\text{RPSEL}}$ and $\overline{\text{WPSEL}}$ control Read and Write to the programmable graphics RAM in G3/G1. Note that pad S (SRD on G7) should be linked to pad S near F3/F4.

Without the "Snow Dinger" the signals $\overline{\text{RPSEL}}$ and $\overline{\text{WPSEL}}$ are linked together via L4 and are connected to an approprate 2K or 4K select output from the mapper - see gates F5 on Fig.4.

When the Z80 generates an address in the field thus mapped, its address lines are routed to the RAM in G3/G1 by the multiplexers G5, G8, G9 and the data lines are connected to the Z80 data bus by G2.

If the "Snow Dinger" is incorporated (and this is highly recommended) the $\overline{\text{RPSEL}}$ and $\overline{\text{WPSEL}}$ signals generated by the "Snow Dinger" connect to pad M and pad E respectively, Link L4 is removed and the 2K/4K-select mapper output connects to the "Snow Dinger" board ($\overline{\text{PGSEL}}$). Complete details of the "Snow Dinger" can be found in Programming Power's magazine "Micropower" issue 1 from page 20 onwards.

Selection of RAM in G3/G1

Two 4118 Static RAM chips, each of 1K by 8 bits, or one 6116 which is 2K by 8 bits, would be fitted in the normal case. This 2K RAM sits above the ROM character generator in terms of character numbering. However, it is possible to fit two 6116 elements and have the second one, at G1, as a switched alternative to the ROM. Under these circumstances a 4K select from the mapper would be necessary to map this into the 64K address field. The links L1 and L2 are connected as for 4118's. Link L3 provides a facility for enabling or disabling the ROM, via G12, i.e. enables the whole of the possible 4K of RAM in G3/G1 or only the top 2K of RAM address. If L3 is connected to 0 volts, as shown in Fig.5, the normal case obtains where the ROM and the 2K of RAM above it, are enabled. If L3 is connected to +5 volts the ROM 2K is disabled and the 4K address field is available for RAM in G3/G1. This can be done physically with a suitable switch or electronically via a port bit.

NASCOM 2 Implementation

NASCOM 2 does not require anything to be fitted at G11 or G12. Also, the inverter gate G6, pin 9 and 8, is not required, so the link N2 should be made with N1 open circuited. The connection from NASCOM 2 to socket G10 must be made with flying leads rather than flat cable and, unlike the NASCOM 1, they are not pin-for-pin. They are as follows:

NASCOM 2 IC54	SIGNAL	PROG	GRAPHICS G10
1	CA3	11	
2	CA2	12	
3	CA1	16	
4	CA0	15	
5	RS3	24	
6	RS2	23	
7	RS1	22	
8	RS0	21	
9	CD0	17	
10	CD1	7	
11	CD2	18	
12	OV	13	
13	CD3	6	
14	CD4	19	
15	CD5	5	
16	CD6	20	
17	CD7	14	
18	GREN	10	
19	CA6	4	
20	GREN	10	
21	+5V	2	
22	CA5	8	
23	CA4	9	
24	+5V	2	

Apart from the special requirements of the NASCOM 2 listed here, the other features described for NASCOM 1 also apply to the NASCOM 2.

Note that G10 pins 1 and 3 carry voltages required by the NASCOM 1 Character Generator, the MCM6576, although in some instances this may be a single-voltage (+5V only) unit fitted in lieu of the original triple-voltage chip.

BUFFER BOARD - Figs.6 and 7

The buffer was designed to interface a NASCOM 1 to NASBUS and at the same time provide some of the extra facilities available on a NASCOM 2.

Extra Facilities

1) Power-on Jump

This facility allows the processor to execute program starting at any preset 4K boundary on power-on or reset. For example, to jump directly to BASIC at switch on.

2) Synchronised Reset

This allows the Reset pulse to be synchronized with processor $\overline{M1}$ cycles. This is necessary so as to prevent corruption of data when using dynamic RAM. The Reset Signal must be a pulse, even if the external reset button is held closed, to avoid suspending the Z80 from refreshing the dynamic RAM, hence losing the data.

3) Wait-State Generator

This allows one wait state to be added to any access, memory or input/output. The input to B12 pin 2 must be linked to the appropriate decode, for example, to $\overline{M1}$ to insert a wait for each instruction fetch, or to $\overline{4KS0}$ to insert a wait on all accesses in the first 4K.

4) ROM Socket

Position B3 has been provided for a 24 or 28 pin ROM or EPROM. By selecting the links at B9 a variety of elements can be used such as 2716, 2732, 2764 or a NASCOM BASIC ROM. Note, however, that only 5 volt, single voltage, units can be used.

5) Input/Output

A partial input/output decode allows for 64 input/output addresses and is provided by B4.

The Data, Address and Control Signal Buffers

The Z80, as used on the NASCOM, will drive only a few external devices. It is necessary, therefore, to add buffering to all signals between the Z80 and NASBUS. The data buffer, B15, is bi-directional thus allows Read (data from the bus) and Write (data to the bus). The direction is determined by the signal $\overline{SEND}$ which is derived from the Z80 $\overline{RD}$ signal at B11, pin 6. The signal SENDI is affected by BUSAK (Bus Acknowledge) and $\overline{INTAK}$ (Interrupt Acknowledge) (B10, pin 11). Because there are addressable devices on the NASCOM 1 (RAM and ROM) the data buffer B15 must be disabled when an access is made to the NASCOM 1. This is done by $\overline{EN}$ at B11, pin 3. The signal $\overline{EN}$ is also affected by BUSAK since it is possible that some external device may also wish to access the NASCOM 1 on-board memory.

The Address Buffers, B16 and B17, are also bi-directional but are left permanently enabled. When the NASCOM 1 is controlling, BUSAK is high, hence the buffers pass the lesser significant 12 bits of the 16-bit address onto NASBUS (pins 30 to 41 inclusive). Note also that B18 is similarly controlled.

Ignoring B8 (Fig.6), it can be seen that the only control for the buffers B7, B16, B17 and B18 is BUSAK and $\overline{\text{BUSAK}}$. When $\overline{\text{BUSAK}}$ is low, due to a second device, say a processor, the buffer will pass addresses from the bus to the NASCOM giving access to the on-board RAM and ROM.

Similarly, the direction control $\overline{\text{SEND}}$ and the enable $\overline{\text{EN}}$ for the data buffers is changed by BUSAK. The exclusive OR-gates generating the signals $\overline{\text{SEND}}$ and $\overline{\text{EN}}$ can be considered as INVERT/NOT INVERT gates with BUSAK as the control signal. Thus, for example, when the NASCOM is reading from the bus, the buffer must be enabled for data from the bus to the NASCOM. When a Direct Memory Access (DMA) device is reading from the bus, the buffer directs data from the NASCOM to the bus but the output is switched off (NASCOM not being accessed). Thus the sense of $\overline{\text{SEND}}$, and therefore the direction of the buffer, is controlled by BUSAK. Element B18 acts as a buffer for control signals from the Z80 and operates in exactly the same way as the address buffer, under the control of BUSAK. The control signals going to the NASCOM are buffered through open-collector gates, such as B19 ($\overline{\text{ZWAIT}}$, $\overline{\text{ZRESET}}$, $\overline{\text{BAO}}$, $\overline{\text{ZBUSRQ}}$ and $\overline{\text{ZINT}}$; note that B19 pins 3 and 4 producing $\overline{\text{WAIT}}$ has R116 as the collector load). These buffers offer protection for the Z80 from possible fault conditions on NASBUS.

Interrupt Operation

There is logic on the buffer board to determine in which direction the data buffers should be enabled during interrupt mode 2. In this mode the Z80 expects data to be placed on the bus by the interrupting device during the Interrupt Acknowledge ($\overline{\text{INTAK}}$) cycle. The signal $\overline{\text{INTAK}}$ is produced by B10 pins 11, 12 and 13 when $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are valid simultaneously. During this period the data buffers allow data from the bus to the NASCOM. This is done by element B11 pin 8 when $\overline{\text{SEND}}$ is gated through the exclusive-OR gate by $\overline{\text{INTAK}}$. This facility can be used only if the interrupting device is on the bus, hence the PIO must be removed from the NASCOM if it is to be used in the interrupt mode 2.

Power-On Jump

Element B8 (see Fig.6) is used to force the top four address lines to the binary value determined by the Restart Address Links on pins 3, 6, 10 and 13, for one $\overline{\text{M1}}$ cycle on receipt of a Reset pulse via MUX on B5 pin 9. Signal M1 on B5 pin 3 causes MUX to reset and B8 connects the top four address lines as normal.

Synchronised Reset

Power-on reset is generated via the network R128, C117 and D1 Signals $\overline{\text{ZRESET}}$ and $\overline{\text{RESET}}$ at B19 pin 2 are held high by the 2.2K resistor to +5V.

When power is applied, C117 is in the discharged state thus holding B13 pin 13 at 0 volts, hence $\overline{\text{RESET}}$ falls to 0 volts. The capacitor C117 charges through R128 and eventually pulls B13 pin 13 up to +5 volts to terminate the $\overline{\text{RESET}}$ pulse.

When the reset switch is pressed, the signal $\overline{\text{RESET SW}}$ is at 0 volts which allows $\overline{\text{M1}}$ to toggle B6 producing a positive-going edge at pin 9. This transition triggers the monostable at B14 which puts a pulse into B13 hence into $\overline{\text{RESET}}$. When the reset

switch is released, B6 is once again cleared thus preventing any further reset pulse being generated.

Input/Output Decode

The NASCOM 1 offers an I/O decode for eight ports. The keyboard uses Port 0, the UART uses Port 1 for data and Port 2 for status and the NASCOM 1 PIO uses Ports 4, 5, 6 and 7. Port 3 is not used.

On NASCOM 1 when INT is selected these devices will also appear at address 8 to 15, 16 to 23, 24 to 31 and so on!

NASCOM 1 I/O decode link should be set to EXT.

The I/O decode at B4 provides a way of decoding eight blocks so that the NASCOM Port addresses will now repeat after 64 addresses instead of 8 as explained above.

If this element (B4) is not fitted, then B4 pin 2 or 14 should be connected to the I/O pad strips on each side of B4. It should be noted that, because of the incompleteness of the NASCOM 1 design, the on-board PIO can no longer be used without modification.

If B4 is fitted, for normal operation, link pin 9 (least significant block) to its adjacent pad on the strip. Also link $\overline{\text{NASIO}}$ to the strip of pads via G (see Fig.1) and H.

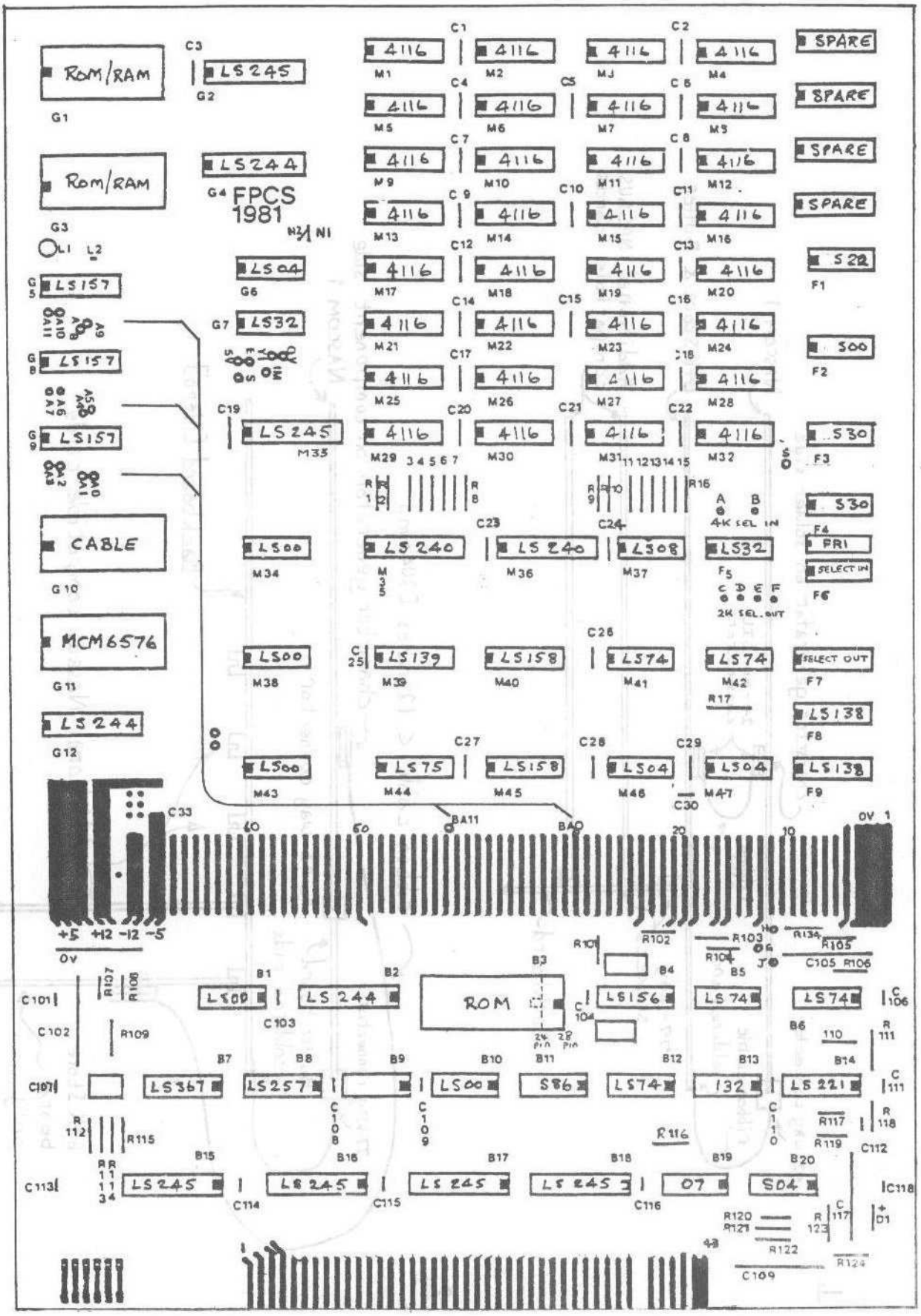
For other decodes, link other pins as required. As mentioned above, pin 9 is the least significant followed by 10, 11, 12, 7, 6, 5 and 4 which is the most significant.

As B4 is an open-collector device, the outputs can be linked together to provide decodes of say 16 or 24 ports if required.

The 43-way/77-way Connectors

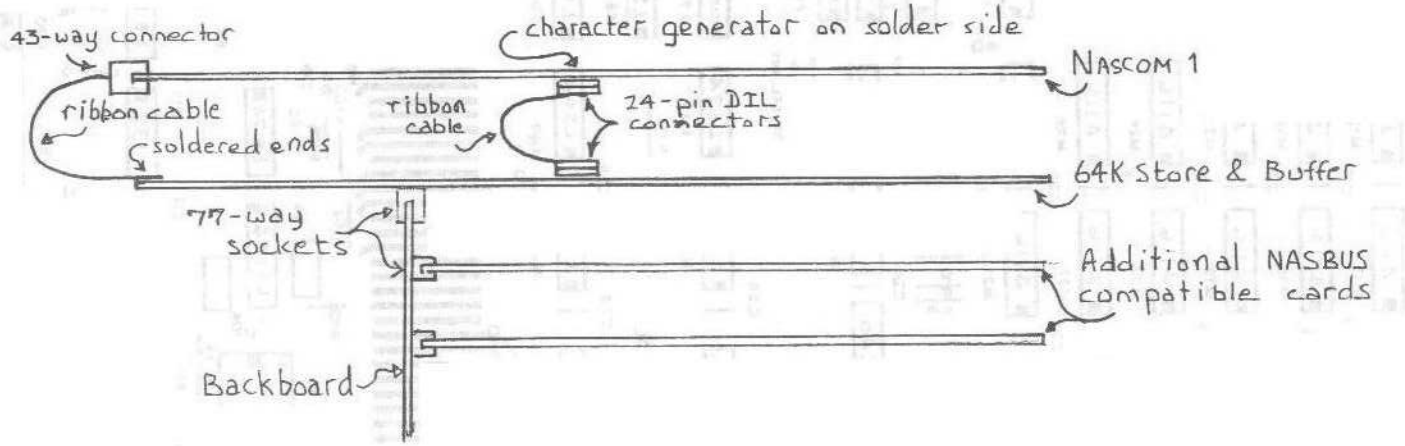
The signal names and corresponding pin numbers for the 43-way NASCOM 1 edge-connector and the 77-way connections are given in Fig.8.

The logic on the buffer card is able to determine the direction of the buffer for all no-fault conditions of bus operation (except for the NASCOM PIO as mentioned above). The signal $\overline{\text{DBDR}}$ (Data Bus Direction), NASBUS pin 13 is therefore redundant for any combination of NASBUS compatible hardware and can be ignored on any system using this buffer card.



Component Layout Fig. 1

1.


43-way connector
character generator on solder side
NASCOM 1
ribbon cable
soldered ends
ribbon cable
24-pin DIL connectors
64K Store & Buffer
77-way sockets
Additional NASBUS compatible cards
Backboard

2.

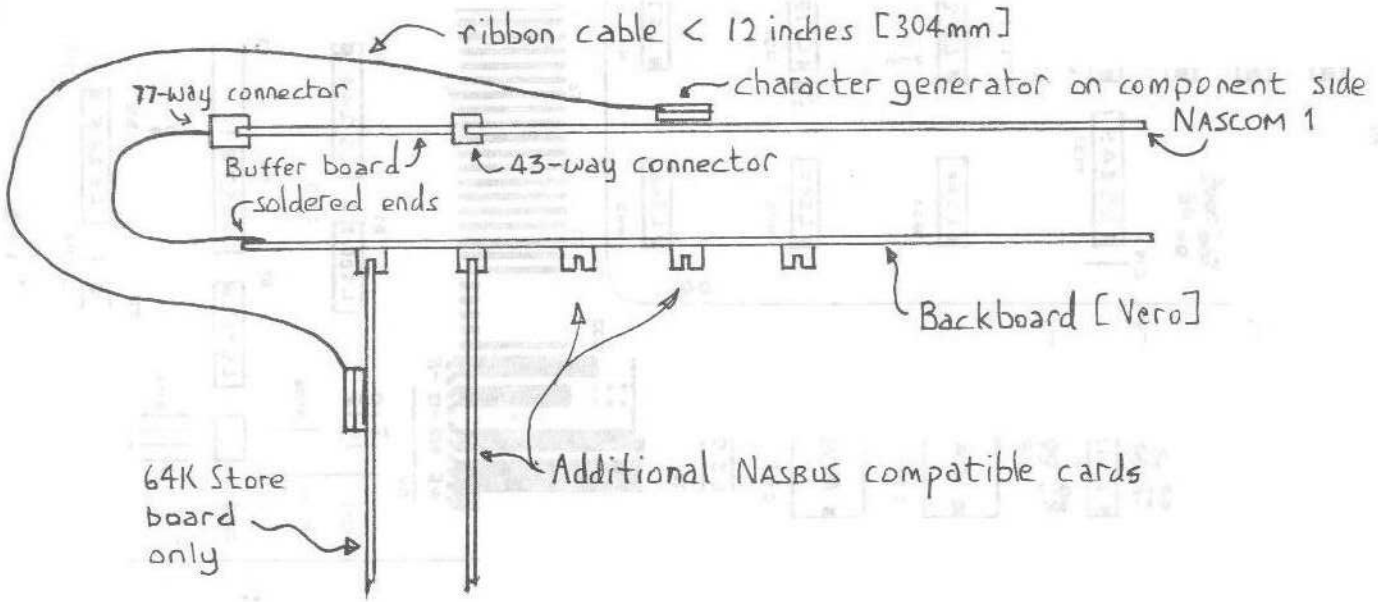
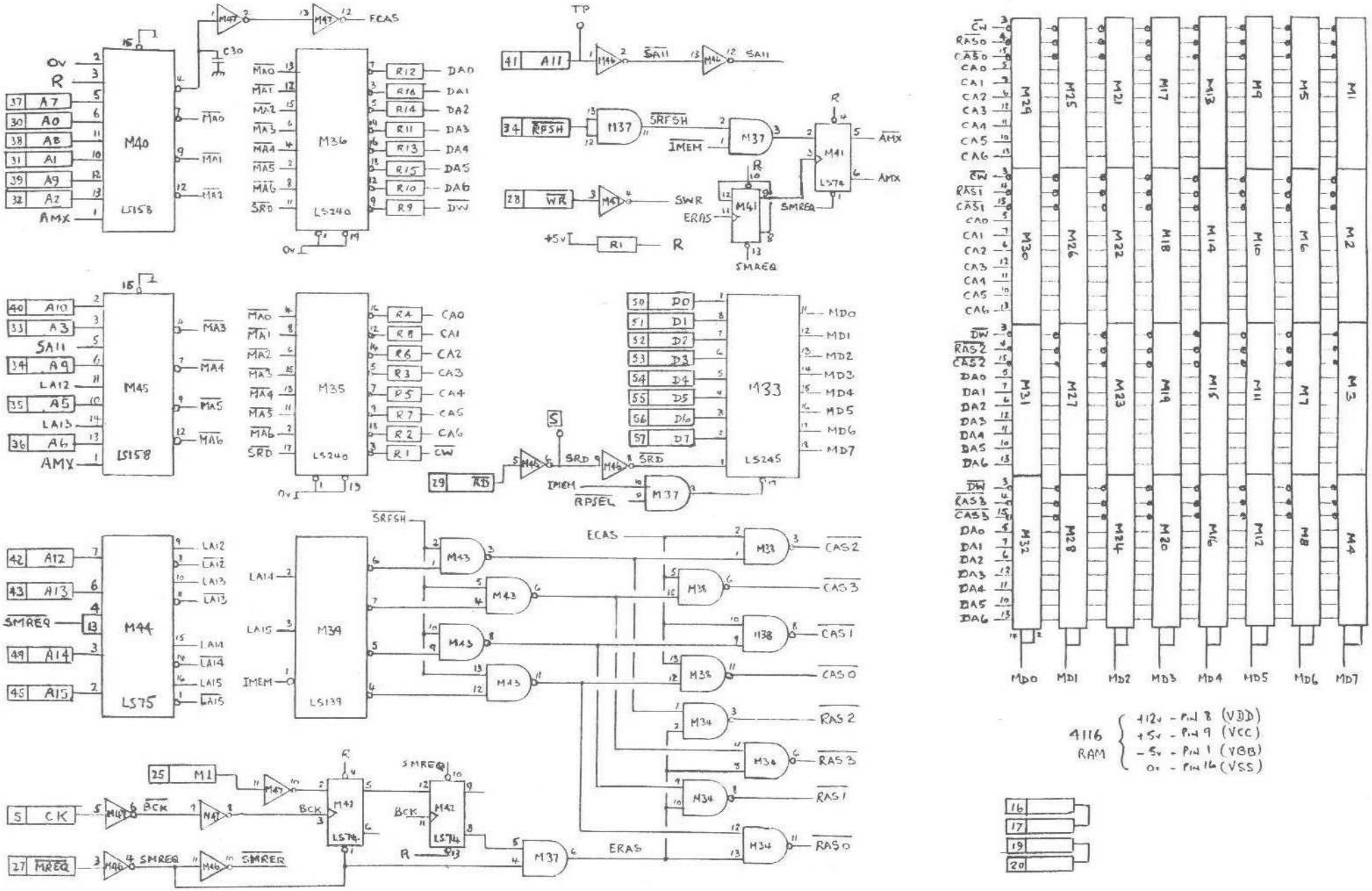
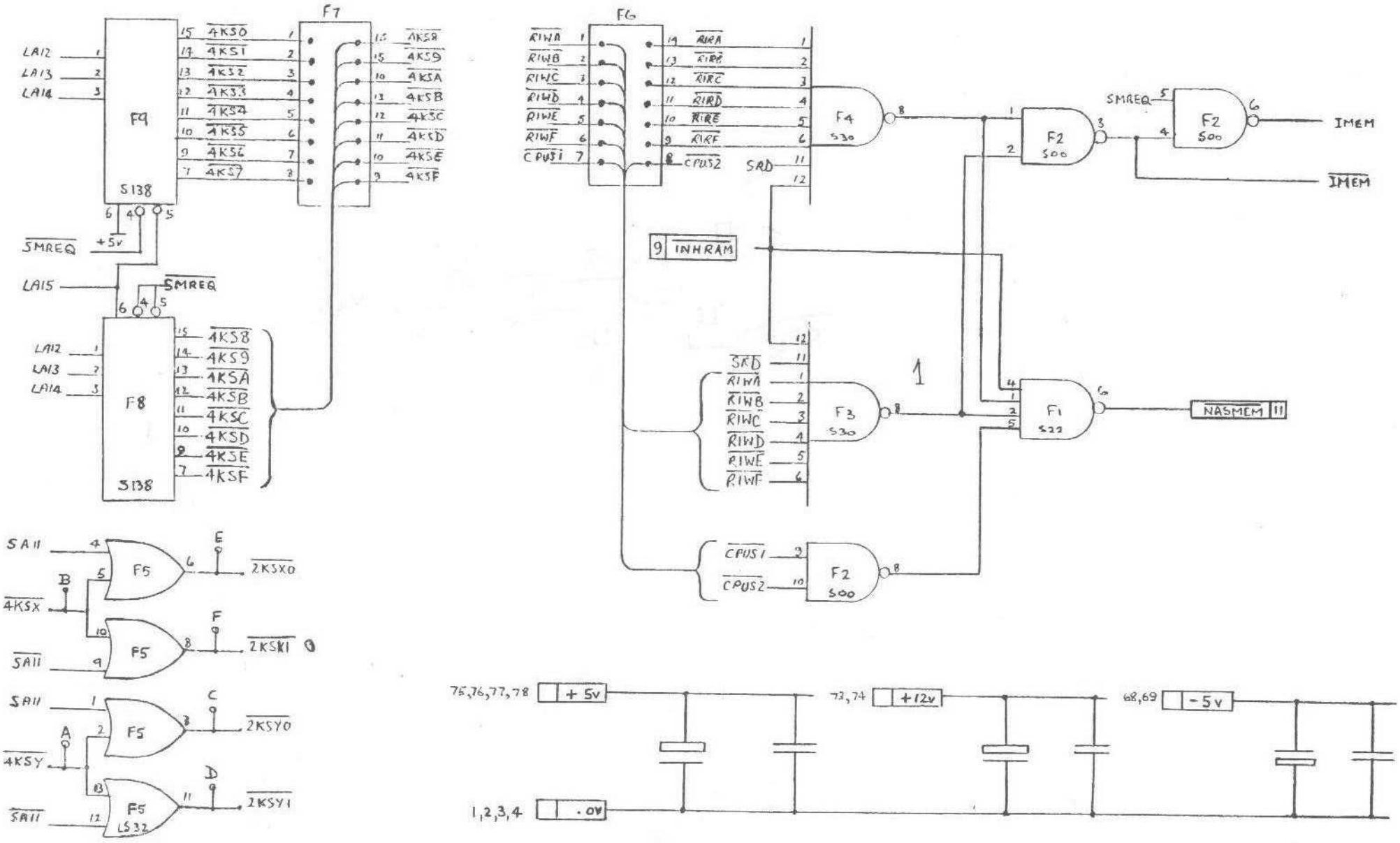

ribbon cable < 12 inches [304mm]
77-way connector
character generator on component side
NASCOM 1
Buffer board
43-way connector
soldered ends
Backboard [Vero]
Additional NASBUS compatible cards
64K Store board only

FIG.2.



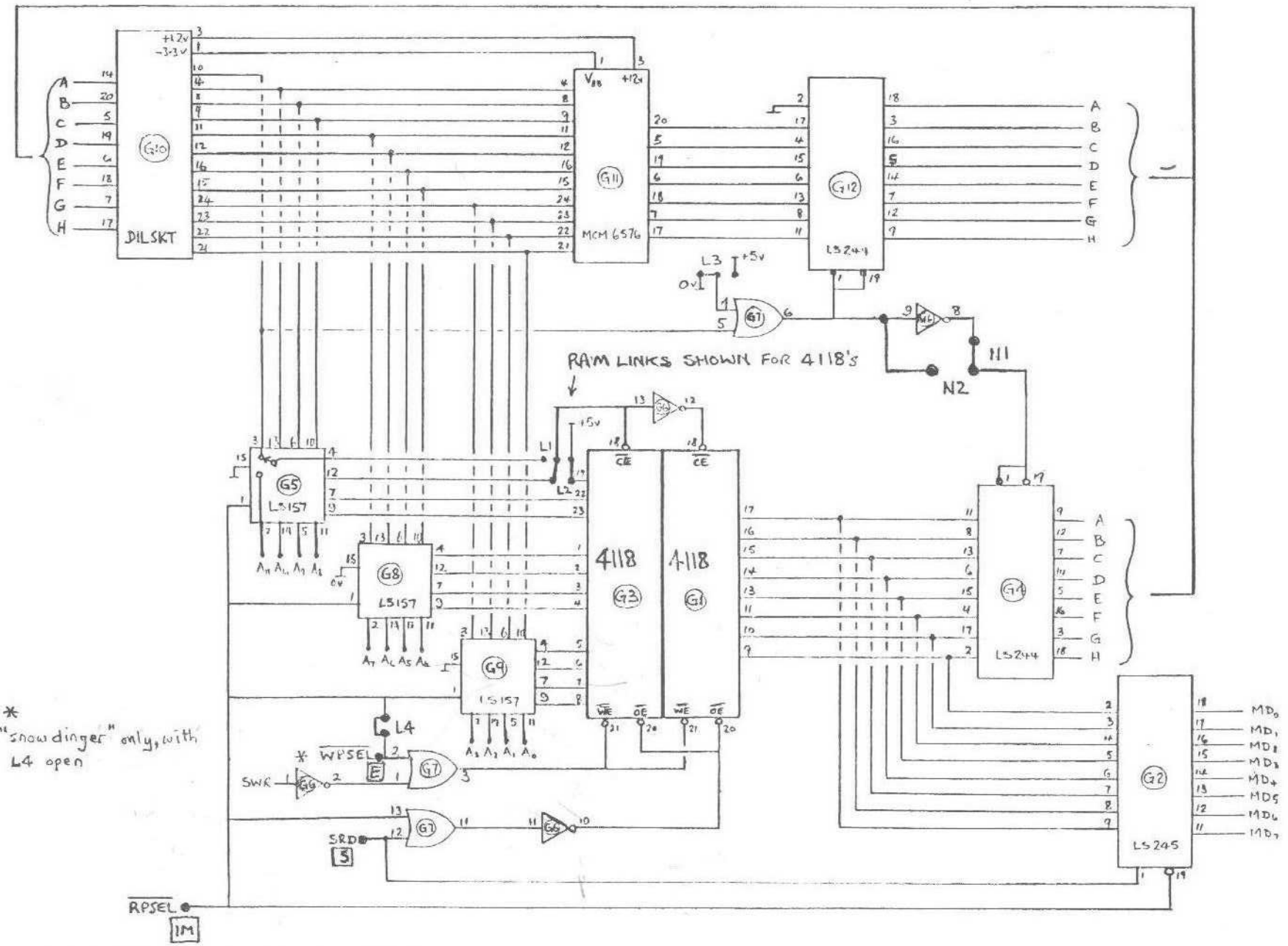
64K RAM & CONTROL LOGIC

FIG.3.



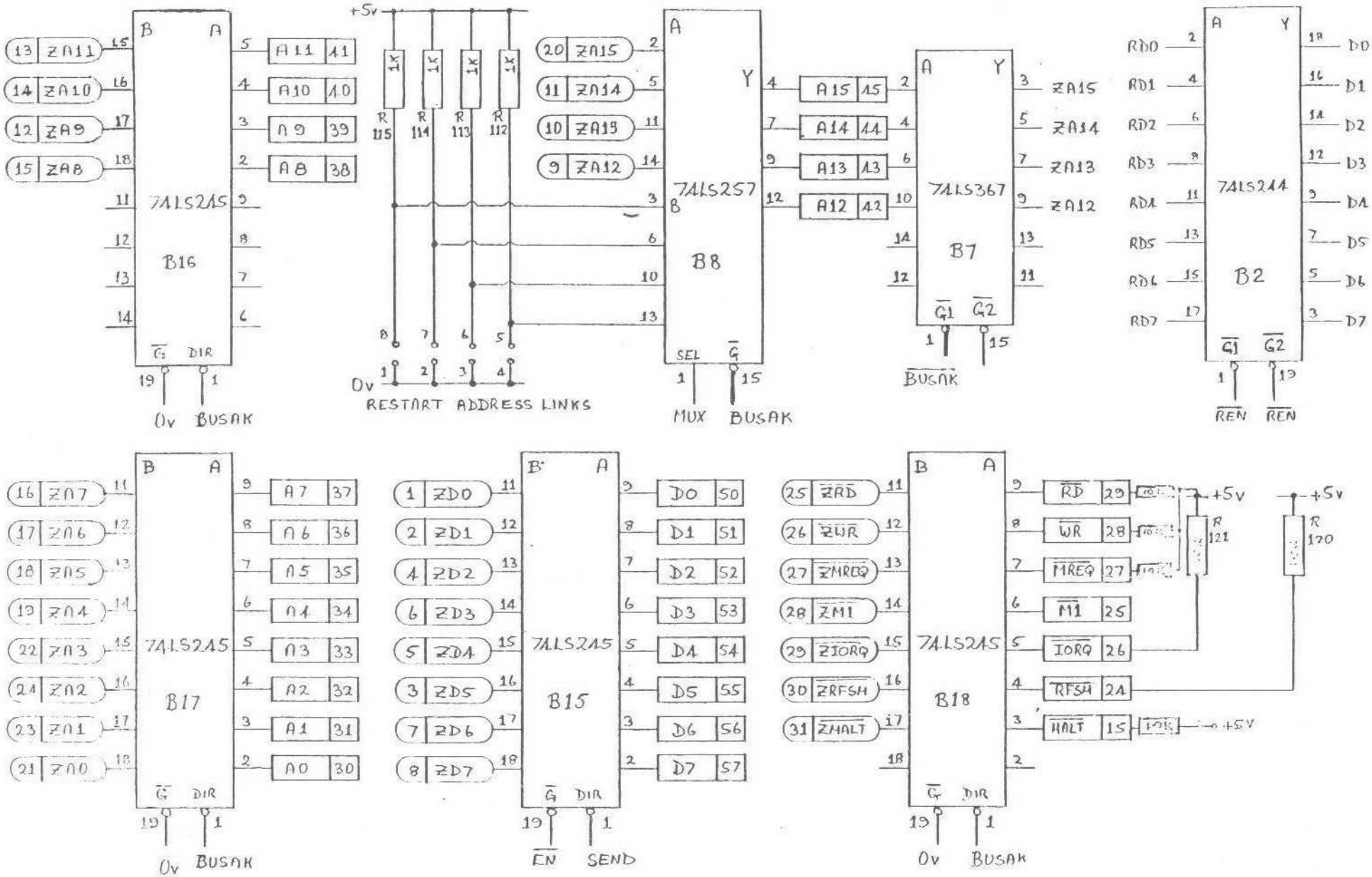
MAPPER LOGIC

FIG.4.



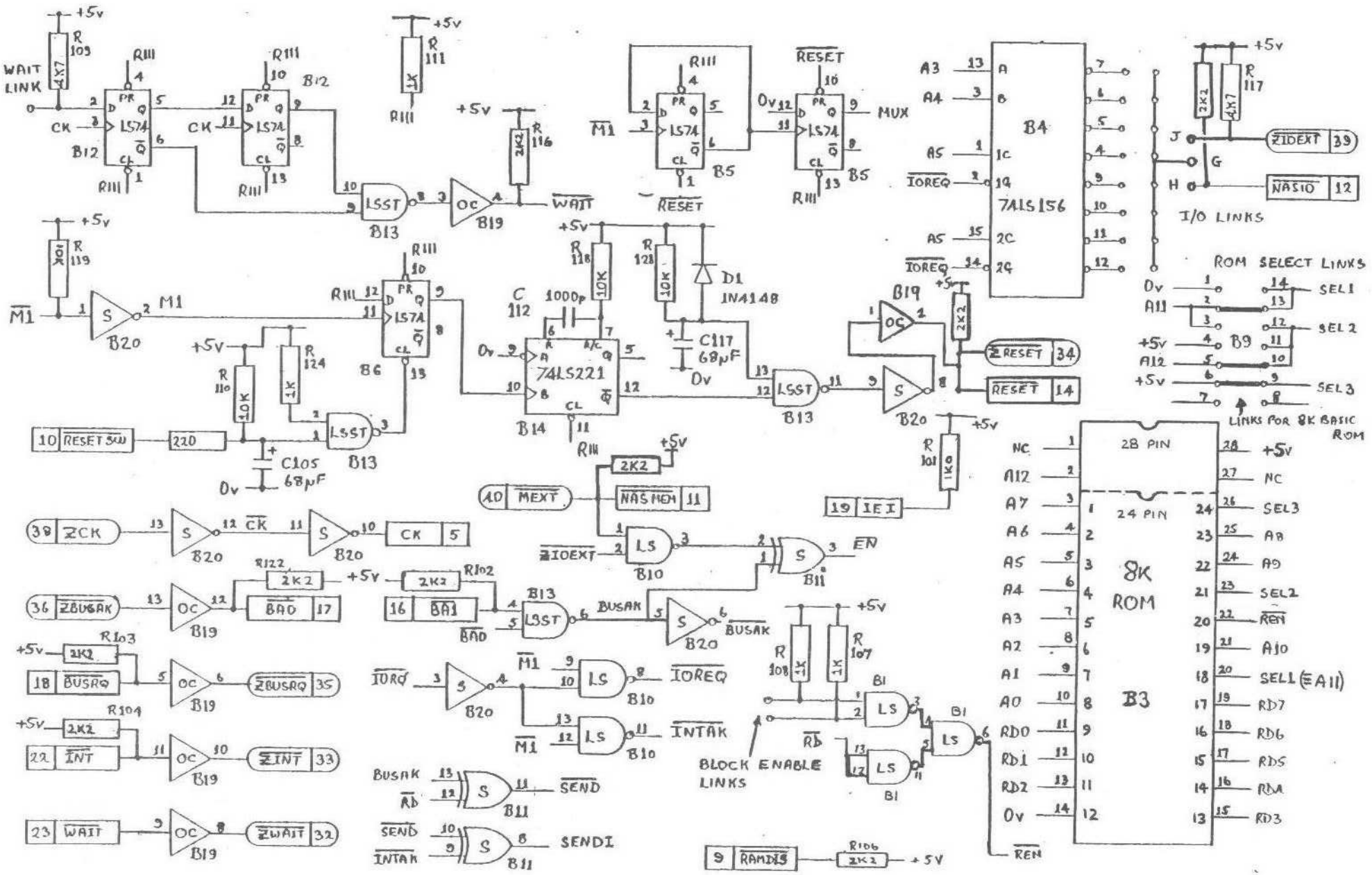
PROGRAMMABLE GRAPHICS LOGIC

FIG.5.



BUFFER LOGIC 1

FIG.6.



BUFFER LOGIC 2

FIG.7.

NASCOM 1	
1	ZD0
2	ZD1
3	ZD5
4	ZD2
5	ZD4
6	ZD3
7	ZD6
8	ZD7
9	ZA12
10	ZA13
11	ZA14
12	ZA9
13	ZA11
14	ZA10
15	ZA8
16	ZA7
17	ZA6
18	ZA5
19	ZA4
20	ZA15
21	ZA0
22	ZA3
23	ZA1
24	ZA2
25	$\overline{\text{ZRD}}$
26	$\overline{\text{ZWR}}$
27	$\overline{\text{ZMREQ}}$
28	$\overline{\text{ZM1}}$
29	$\overline{\text{ZIORQ}}$
30	$\overline{\text{ZRFSH}}$
31	$\overline{\text{ZHALT}}$
32	$\overline{\text{ZWAIT}}$
33	$\overline{\text{ZINT}}$
34	$\overline{\text{ZRESET}}$
35	$\overline{\text{ZBUSRQ}}$
36	$\overline{\text{ZBUSAK}}$
37	KEYWAY
38	ZCK
39	$\overline{\text{ZIOEXT}}$
40	MEXT
41	+5v
42	0v
43	0v

NASBUS EDGE CONNECTOR			
1	0v	41	A11
2	0v	42	A12
3	0v	43	A13
4	0v	44	A14
5		45	A15
6		46	
7		47	
8		48	
9	$\overline{\text{RAMDIS}}$	49	
10	$\overline{\text{RESETSW}}$	50	D0
11	$\overline{\text{NASMEM}}$	51	D1
12	$\overline{\text{NAS IO}}$	52	D2
13		53	D3
14	$\overline{\text{RESET}}$	54	D4
15	$\overline{\text{HALT}}$	55	D5
16	$\overline{\text{BAI}}$	56	D6
17	$\overline{\text{BAO}}$	57	D7
18	$\overline{\text{BUSRQ}}$	58	
19	IEI	59	
20	IEO	60	
21		61	
22	$\overline{\text{INT}}$	62	
23	$\overline{\text{WAIT}}$	63	
24	$\overline{\text{RFSH}}$	64	
25	$\overline{\text{M1}}$	65	
26	$\overline{\text{IORQ}}$	66	
27	$\overline{\text{MREQ}}$	67	
28	$\overline{\text{WR}}$	68	-5v
29	$\overline{\text{RD}}$	69	-5v
30	A0	70	-12v
31	A1	71	-12v
32	A2	72	KEYWAY
33	A3	73	+12v
34	A4	74	+12v
35	A5	75	+5v
36	A6	76	+5v
37	A7	77	+5v
38	A8	78	+5v
39	A9		
40	A10		

SIGNALS ON THE LOGIC DIAGRAM
THUS ( ) REFER TO NASCOM 1 CONNECTOR
AND [ ] REFERS TO NASBUS CONNECTOR

THE 43-WAY/77-WAY CONNECTORS FIG.8.